Remarks/Arguments

Claims 20-38 are pending in the present application.

Claim Rejections – 35 U.S.C. 112

Claims 20 and 23 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The Examiner has asserted that claim 20 fails to clearly feature which register is selectively connected to the input/output circuit, because both a write register and a read register are featured in claim 20. This rejection is respectfully traversed for the following reasons.

The serial access memory of claim 20 includes in combination a write register, a read register and an "input/output circuit selectively connected to the registers". Although not necessarily limited thereto, and as considered herein merely for the purpose of explanation, the input/output circuit of claim 20 may be interpreted collectively as input circuit L and output circuit M illustrated in Figs. 1A and 1B, for example. Write registers WRm and read registers RRm may be considered as both selectively coupled to the input/output circuit L and M. Accordingly, Applicant respectfully submits that claims 20 and 23 particularly point out and distinctly claim the subject matter of the invention, and thus are in compliance with 35 U.S.C. 112, second paragraph. The Examiner is therefore respectfully requested to withdraw this rejection for at least these reasons.

Claim Rejections – 35 U.S.C. 102

Claims 20-38 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Iwamoto et al. reference (U.S. Patent No. 5,592,434). This rejection is respectfully traversed for the following reasons.

The serial access memory of claim 20 includes in combination "a pair of column lines selectively connected to the first bit lines or the second bit lines, the column lines being located substantially parallel with the first and second bit lines"; and a control circuit "selectively connecting the column lines with the first bit lines or the second bit lines". Applicant respectfully submits that the Iwamoto et al. reference as relied upon by the Examiner does not disclose these features.

The Examiner has interpreted lines CSL and CSL' in Fig. 2 of the Iwamoto et al. reference as the pair of column lines of claim 20, and transistors CSG2 and CSG2' as the control circuit of claim 20.

However, as described in column 15, lines 23-33 of the Iwamoto et al. reference, column selecting gate CSG2 connects bit lines pairs BLP of each column to local IO line pair LIO2, and column selecting gate CSG2' connects bit line pairs BLP of each column to local IO line pair LIO2'. Column selection lines CSL are arranged corresponding to column selecting gate CSG2, and column selection lines CSL' are arranged corresponding to column selecting gate CSG2'. The circuit for selecting column selection lines CSL and CSL' is shown in Fig. 3.

Accordingly, lines CSL and CSL' in Fig. 2 of the Iwamoto et al. reference are

column selection lines, not column lines as alleged by the Examiner. Particularly, column selecting gates CSG2 and CSG2' couple bit lines pairs BLP respectively to local IO line pairs LIO2 and LIO2'. Column selection lines CSL and CSL' in Fig. 2 of the Iwamoto et al. reference are not selectively connected to bit line pairs BLP, and thus cannot be interpreted as the column lines of claim 20. Moreover, column selecting gates CSG2 and CSG2' in Fig. 2 of the Iwamoto et al. reference do not selectively couple bit line pairs BLP to column lines, and more particularly do not couple bit line pairs to column lines that are located substantially parallel with respect to bit lines, as would be necessary to meet the features of claim 20. Accordingly, Applicant respectfully submits that the serial access memory of claim 20 distinguishes over the Iwamoto et al. reference as relied upon by the Examiner, and that this rejection of claims 20-26 is improper for at least these reasons.

The serial access memory of claim 27 includes in combination a column line "selectively connected to one of the first bit lines or one of the second bit lines, the column line being located substantially parallel with the first and second bit lines"; and a control circuit "selectively connecting the column line with the one of the first bit lines or the one of the second bit lines". Applicant respectfully submits that column select lines CSL and CSL', and column selecting gates CSG2 and CSG2' in Fig. 2 of the Iwamoto et al. reference cannot respectively be interpreted as the column line and the control circuit of claim 27, for at least somewhat similar reasons as set forth above. Accordingly, Applicant respectfully submits that the serial access memory of claim 27

distinguishes over the Iwamoto et al. reference as relied upon by the Examiner, and that this rejection of claims 27-32 is improper for at least these reasons.

The serial access memory of claim 33 includes in combination a plurality of column lines "selectively connected to one of the first bit lines or one of the second bit lines, the column lines being located substantially parallel with the first and second bit lines"; and a control circuit "selectively connecting one of the column lines with one of the first bit lines or the second bit lines". Applicant respectfully submits that the serial access memory of claim 33 distinguishes over the Iwamoto et al. reference as relied upon by the Examiner, and that this rejection of claims 33-38 is improper for at least somewhat similar reasons as set forth above.

Conclusion

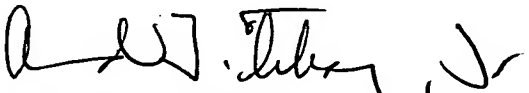
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.



Andrew J. Telesz, Jr.
Reg. No. 33,581

Tel. No. (703) 715-0870
Fax No. (703) 715-0877